

PLANAR ULTRA VIOLET LIGHT DETECTOR

Background

The present invention relates to sensors and particularly
5 to ultra violet light (UV) detectors. More particularly, the
invention relates to detecting UV from various sources of light.

Successful related art UV detectors have been primarily
based on highly specialized processes built around "vacuum" tube
technology. The physics of such detectors are that the tube of
10 each detector may have a cathode electrode such as tungsten or
copper which is the surface from which optically excited
electrons are originated, and an anode grid that lets light pass
through it but is charged such that it will collect electrons
generated by the breakdown instigated by the photoemission of an
15 electron at the cathode surface. The tube may be filled with a
neon/hydrogen (Ne/H₂) gas mixture to facilitate the breakdown
nominally at about 100 Torr residual pressure. Several factors
that appear to define and limit device yield and performance may
include tube glass cleanliness, gas mixture, plate spacing and
20 gas contamination. These potential causes of problems may be
eliminated or minimized with the present invention.

Summary

The present invention is a wafer-based UV detection device. It is effectively a micro-machined Geiger-Mueller tube type structure based on micro-fabrication processes, such as the new 5 MEMS and silicon integrated current fabrication technology with wafer-scale batch processes. The silicon device may be a "mini tube" having equal or better performance, significantly smaller size and lower cost than the related art UV sensing tubes. The present device may involve an assembly of three wafers. They 10 include a lower silica cathode wafer, an intermediate fused silica spacer/plasma wafer having a volume of space, and a top silica mode wafer. A "tube" chamber may exist between the top and bottom wafers. The chamber may be situated between the anode and cathode. The device may be an all-fused silica wafer 15 stack. There may be various configuration permutations in the mask layout used for fabricating the wafer-based detection device, which may affect performance, yield and lifetime of the device.

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Brief Description of the Drawings

Figure 1 shows relative voltage levels for UV tube operation;

Figure 2 is a cross-section view of a wafer-based UV light detection device;

Figure 3 shows a plan view of the detection device revealing the anode grid;

5 Figure 4 shows a wafer with numerous devices prior to dicing;

Figures 5a, 5b, 5c, 5d and 5e identify a chamber diameter, the cathode diameter, the anode opening size, the anode mesh size and the seal gap between cathode and spacer wafers of the
10 UV detection device, respectively;

Figures 6a and 6b are a cross-section view and top view, respectively, of the etched moat in the cathode wafer;

Figures 7a and 7b show a deposit of cathode metal and a eutectic layer;

15 Figures 8a and 8b show the removal of the eutectic layer to expose the cathode metal;

Figures 9a and 9b reveal the patterned street features on the back of the cathode wafer;

Figures 10a and 10b show the spacer wafer with a layer of
20 metal on the front and back of it;

Figures 11a and 11b show the spacer wafer with alignment marks for drilling;

Figures 12a and 12b reveal anode metal and eutectic layers on the anode wafer;

Figures 13a and 13b show the exposure of the anode metal with the unmasked portion of the eutectic layer removed;

5 Figures 14a and 14b illustrate the pattern and etch of the anode grid on the anode wafer;

Figures 15a and 15b reveal a contact hole for an external connection to the cathode;

10 Figures 16a and 15b show the drilled chamber hole of the spacer wafer;

Figures 17a and 17b reveal a contact hole for an external connection to the anode;

Figures 18a and 18b illustrate the eutectic bonding of the cathode wafer and the spacer wafer; and

15 Figures 19a and 19b illustrate the eutectic bonding of the anode wafer to the spacer wafer resulting in a three wafer bonded assembly of numerous "mini-tube" detectors.

Description

20 Figure 1 reveals relative voltage ranges for a UV tube operation. Voltage range 11 shows a plasma discharge in the tube without the presence of UV light. Range 12 is where the

breakdown voltage starts and voltage 15 is where the discharge stops without UV. Voltage 16 is the voltage starting level with UV. In voltage range 14, between voltages 17 and 16, the discharge may be sustained in the presence of UV light but will 5 not start in the absence of UV. A voltage in range 15 below the discharge sustaining voltage 17, there is no discharge even in the presence of UV light. Region 18 may be in a desired operating voltage range for UV tube operation.

Figure 2 is a cross-section view of the wafer-based UV 10 light detection mini tube or device 20. The three wafers that may be the structural basis of sensor or detector 20 include a silica cathode wafer 21, a silica spacer wafer 22 and a silica anode wafer 23. Other appropriate materials, particularly those with similar temperature coefficients of expansion, may be used 15 in lieu of silica for one or more of wafers 21, 22 and 23. Formed on wafer 21 may be a cathode metal 24 and on wafer 23 may be an anode metal 25. Space wafer 22 is a support between wafers 21 and 23 to provide a discharge or plasma "tube-like" 20 space, cavity or chamber 26 for detector 20. Figure 3 reveals a grid-like appearance of anode 25. Numerous detectors 20 may be fabricated together on wafer combination 27 of several inches in diameter as shown in Figure 4. Wafer combination 27 may be

diced into individual detector 20 chips or groups of detector 20 chips.

Various dimensions of detector 20 may include cathode 24 size, anode 25 size, anode mesh size, the gap between the anode 5 feature on the top anode wafer 23 and the chamber 26 hole in the fused silica wafer 22. Figure 5a shows that the diameter 28 of chamber 26 may be 5 or 9 millimeters (mm). Diameter 28 may be chosen to be consistent with the standard tube cathode 24 area. The photo cathode 24 metal platform of figure 5b may have a 10 diameter 29 of 4, 5.6 or 8 mm. One may chose the smaller cathode and anode to increase die leverage for better cost per chip. Figure 5c notes that the ratio of anode 25 opening 31 area to the cathode 24 opening 29 area may vary from 1:1 to 0.5:1. This parameter may aid in an understanding of the 15 interaction between a spacer silica 22 hole size 28 and an anode 25 size 31 and cathode 24 size 29. In figure 5d, anode 25 may have a mesh size width 31 of 10 microns or 50 microns. This parameter may influence the anode 25 life as well as its transmission behavior. Figure 5e notes cathode silica to spacer 20 silica seal gap 33. Gap 33 may have a width of 100, 200 or 400 microns. This parameter may be used to control potential electrical leakage due to sputter deposition.

A process sequence may be used in making detector 20. Even though the ensuing steps in this description are related to only one detector device 20, the effects of the steps may be multiplied by the number of devices 20 on the wafers because the 5 steps may be applied to whole wafer of potential devices 20. The order of the steps may be varied. Other steps may be added. Some steps may be skipped or deleted. Also, what constitutes a step may be changed. The materials mentioned in the present description are merely illustrative examples as other materials 10 may be appropriate for the structure of the present invention.

In the first step, a moat 34 may be patterned in cathode wafer 21 using LAM or a glass etcher. Moat 34 depth may be a parameter for splits. A first mask may be used for the pattern in etching wafer 21. This step is shown in the cross-section 15 view of Figure 6a and the top view of Figure 6b.

The second step may include depositing tungsten (W) cathode 24 material over the whole of wafer 25 at a maximum thickness, followed by 5000 angstroms of sputtered silicon as a eutectic layer 35. Other materials may be used for cathode 24. The 20 cross-section and top views of this step are shown in Figures 7a and 7b, respectively.

In step three, a second mask may be used to pattern eutectic layer 35 on cathode wafer 21 to expose W cathode 24 surfaces as well as open alignment 36 for wafer drilling alignment. Alignment marks 36 may be aligned to moat cut 34.

5 This step is shown in Figures 8a and 8b.

For step four, 200 angstroms of titanium-tungsten (TiW) may be deposited on the back of wafer 25 (not shown). Using a third mask, one may pattern street features 37 and wafer bonder marks on the back side of cathode wafer 25 for visual references. One 10 may align front to back using standard masks. One thousand angstroms of sputtered silicon nitride (Si_3N_4) may be deposited on the back to passivate the TiW in the bonder marks (not shown). Streets 37 are shown in Figures 9a and 9b.

In step five, 1000 angstroms of TiW and 6 microns of gold 15 (Au) may be deposited on the top side of gap wafer 22. In step six, 1000 angstroms of TiW and 6 microns of Au may be deposited on the bottom side of gap wafer 22. The six microns of gold in the eutectic bonding layer on the top and bottom surfaces of gap or spacer wafer 22 may accommodate flatness discrepancies 20 between wafer 22 and wafers 23 and 21, respectfully. These depositions are represented by layers 38 and 39 in figures 10a and 10b. Further, a thin layer of gold or like material may be

deposited on the surface of each wafer (21, 22 and 23) where other bonding material is to be applied for the purpose of a bonding to another wafer. In step seven, the top side of gap wafer 22 may be patterned with a flag clearing mask (i.e., the 5 fourth mask). Likewise, the bottom side of wafer 22 may be patterned. Then layers 38 and 39 of Au and TiW may be wet etched in areas 41 and 40, respectively, as shown by figure 11a. Figure 11b shows the top side of etched layer 38.

For step eight, 5000 angstroms on Ni may be deposited on 10 the bottom side of anode wafer 23, followed by a deposit of 5000 angstroms of silicon (Si) or the like, as indicated by layers 25 and 42, respectively. A nickel (Ni) layer 25 may be the anode material. Other materials may be used in lieu of Ni. The Si deposition may be for a eutectic layer 42. Figures 12a and 12b 15 show this step.

For step nine, a fifth mask may be used to pattern an anode seal feature. The mask pattern may be centered as well as possible. Etching may be used to remove the unmasked portion of eutectic layer 42. Anode layer 25 of Ni functions as an etch 20 stop in this step. The step result is shown in a cross-section view in figure 13a and a top view in figure 13b.

In step ten, an anode grid feature with dimension 32 may be patterned with a sixth mask on Ni layer 25 of wafer 23. The pattern of the sixth mask may be aligned with the eutectic layer cut of the fifth mask. The etching of the pattern into the 5 nickel may result in anode grid 25. Figures 14a and 14b reveal the resultant anode grid 25.

In step 11, cathode wafer 21 may have a contact hole 43 drilled, as shown in figures 12a and 12b (top view). The hole may be 1 mm in diameter for a contact from outside wafer 21 to 10 cathode 24. The hole is shown in figures 15a and 15b. An external contact connection to cathode 24 may be placed through hole 43.

In step 12, spacer wafer 22 may have a 5 mm or 9 mm chamber hole drilled and/or machined to obtain space 26 between cathode 15 24 and anode 25 after assembly of detector 20. The resulting hole, chamber or space 26 in spacer wafer 22 is shown in figures 16a and 16b.

In step 13, a 1 mm hole 44 may be drilled in anode wafer 23 for providing contact to anode 25 from outside of wafer 23. 20 Hole 44 is shown in figures 16a and 16b (bottom view). An external contact connection to anode 25 may be placed in hole 44.

Step 14 may include bringing eutectic bond silicon surface 35 of cathode wafer 21 to bottom Au layer 39 of spacer wafer 22 in a bonder but ensuring that the Au surface of layer 39 does not touch the silicon carbide (SiC) chuck. First, wafer 21 may 5 be put in the bonder with cathode 24 facing down. An image may be captured and then wafer 22 may be put in the bonder with the patterned gold face down (flag zones). The alignment masks between the cathode cut and flag clear the cut. Contact between patterned layers 39 and 35 may result in a eutectical bonding of 10 wafers 22 and 21. These bonded wafers are shown in figures 18a and 18b (top view).

Step 15 may involve aligning and baking out the cathode wafer 21/spacer wafer 22 bonded pair before the final eutectic bond with anode wafer 23, and backfilling with 15 percent 15 hydrogen and 85 percent neon gas. To eutectically bond anode wafer 23 to the bonded pair of wafers 21 and 22, one may load anode wafer 23 first with the anode 25 features face down. Then one may align and capture an image, load the bonded wafer 21/22 pair with the wafer 21 face down and the TiW/Au surface of layer 20 39 face up. The marks on the back of wafer 21 may be aligned to the captured image. The flags are pulled to form the eutectic bond of wafers 22 and 23 upon contact of areas of layers 38 and

42, resulting in a bonded triple wafer of wafers 21, 22 and 23.

For step 16, the bonded wafers may be sawed or diced into separate chips or devices 20. Then the devices may be tested.

Although the invention has been described with respect to 5 at least one illustrative embodiment, many variations and modifications will become apparent to those skilled in the art upon reading the present specification. It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations 10 and modifications.